

Applicant : Tianqiong Liu et al.
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REMARKS

Claims 1-18 were pending of which claims 1 and 14-18 are independent. Claims 1 and 13-18 are amended for clarity. Claims 19 and 20 are added. No new matter is added. Reconsideration of the action mailed July 12, 2005, is requested in light of the foregoing amendments and the following remarks.

The Examiner rejected claims 1-3, 5, 12, and 15-18 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,607,313 to Farries et al. (hereinafter "Farries") in view of U.S. Patent No. 6,724,994 to Collings et al. (hereinafter "Collings"). The Examiner rejected claims 4 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Farries in view of Collings and further in view of U.S. Patent No. 6,271,952 to Epworth (hereinafter "Epworth"). The Examiner rejected 7-11 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Farries in view of Collings and further in view of U.S. Patent No. 4,768,848 to Vaerewyck (hereinafter "Vaerewyck"). The Examiner rejected claim 13 under 35 U.S.C. § 103(a) as being unpatentable over Farries in view of Collings and further in view of U.S. Patent No. 5,111,322 to Bergano et al. (hereinafter "Bergano"). Applicant respectfully traverses the rejections.

Section 103 Rejections

Claim 1 stands rejected as unpatentable over Farries in view of Collings. Claim 1 is directed to an optical time division multiplexing module that includes an integrated time-delay chip. The integrated time-delay chip includes a plurality of waveguides formed on a substrate of the integrated time-delay chip for introducing an optical delay and for combining optical Return-to-Zero signal streams where the optical Return-to-Zero signal streams are combined including interleaving the plurality of waveguides on the integrated time-delay chip.

The Examiner states that Farries fails to disclose an integrated chip that includes a plurality of waveguides, but that Collings does at col. 5, lines 12-52. Applicant respectfully disagrees. The cited section of Collings discloses a multiplexing system. The multiplexing system includes a plurality of lasers coupled to a plurality of modulators for providing separate

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modulated signal streams. *See* FIG. 3; col. 5, lines 12-18. The modulators are coupled to a combiner using optical fibers of varying lengths. *See* FIG. 3; col. 5, lines 19-34. The different optical fiber lengths allow a delay to be provided to the respective modulated signals. *See* FIG. 3; col. 5, lines 26-52. The combiner apparatus then multiplexes the modulated signals to a single output fiber. *See* FIG. 3; col. 5, lines 53-65.

Collings does not disclose or suggest an integrated chip which includes a plurality of waveguides formed on a substrate of the integrated time-delay chip, which provide both a time delay and combining of optical signals within the chip. Thus, the waveguides formed on the chip substrate provide a time-delay and combine the optical signals. (The Applicant notes that the claim is not directed to an integrated time-delay, as indicated by the Examiner, but an integrated chip which provides a time-delay.) In Collings, distinct components are coupled using optical fibers; Collings does not provide an integrated chip that provides both the delay and combining functions within a single chip structure. Instead, Collings discloses a system of discrete components linked together by optical fibers.

Furthermore, Collings does not disclose or suggest waveguides formed on a substrate of a time-delay chip. Therefore, Collings does not disclose or suggest combining the optical streams by interleaving a plurality of waveguides on an integrated time-delay chip. The combining of the optical streams in Collings is provided by a separate combiner component. Collings does not disclose or suggest combining the optical signals by interleaving the plurality of waveguides, which are formed on a substrate of the integrated chip, as required by claim 1. Applicant respectfully submits that claim 1, as well as claims 2-13, which depend from claim 1, are in condition for allowance.

Claim 14 stands rejected over Farries in view of Collings. Claim 14 is directed to a multiplexing module that includes an integrated time-delay chip having a plurality of waveguides formed on a substrate of the integrated time-delay chip.

The Examiner states that Farries does not disclose an integrated time-delay chip having a plurality of waveguides. Collings also fails to disclose or suggest a plurality of waveguides formed on a substrate of an integrated time-delay chip. As discussed above with respect to claim

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1, Collings discloses a plurality of modulators coupled to a combiner through a set of optical fibers. However, Collings fails to disclose or suggest an integrated time-delay chip which has a plurality of waveguides formed on the time-delay chip. Collings does not disclose or suggest a time-delay chip providing a substrate or other structure upon which waveguides can be formed. Furthermore, Collings fails to disclose or suggest waveguides formed on a chip substrate where the waveguides provide a delay between optical signals and where the waveguides are interleaved in order to combine the optical signals. Applicant respectfully submits that claim 14, as well as claim 19, which depends from claim 14, are in condition for allowance.

Claim 15 stands rejected over Farries in view of Collings. Claim 15 is directed to a multiplexing module that includes an integrated time-delay chip that includes first and second waveguides formed on a substrate of the integrated time-delay chip. For the reasons set forth above with respect to claim 14, claim 15 as well as claim 20, which depends from claim 15 are in condition for allowance.

Claim 16 stands rejected over Farries in view of Collings. Claim 16 is directed to a multiplexing module that includes an integrated time-delay chip that includes first and second waveguides formed on a substrate of the integrated time-delay chip. For the reasons set forth above with respect to claim 14, claim 16 is in condition for allowance.

Claim 17 stands rejected over Farries in view of Collings. Claim 17 is directed to a multiplexing module that includes an integrated time-delay chip that includes first and second waveguides formed on a substrate of the integrated time-delay chip. For the reasons set forth above with respect to claim 14, claim 17 is in condition for allowance.

Claim 18 stands rejected over Farries in view of Collings. Claim 18 is directed to an optical time division multiplexing module that includes an integrated time-delay chip. The integrated time-delay chip includes a plurality of waveguides formed on a substrate of the integrated time-delay chip for introducing an optical delay and for combining optical Return-to-Zero signal streams where the optical Return-to-Zero signal streams are combined by interleaving the plurality of waveguides on the integrated time-delay chip. For the reasons set forth above with respect to claim 1, claim 18 is in condition for allowance.

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Pursuant to 37 CFR §1.136, applicant hereby petitions that the period for response to the action dated July 12, 2005, be extended for one month to and including November 14, 2005.

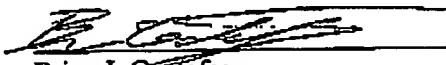
Kindly note November 12, 2005 falls on a Saturday, defaulting the due date to Monday, November 14, 2005

Please apply \$120 for the required extension of time fee to Deposit Account No. 06-1050.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 14 November 2005


Brian J. Gustafson
Reg. No. 52,978

Fish & Richardson P.C.
500 Arguello Street, Suite 500
Redwood City, California 94063
Telephone: (650) 839-5070
Facsimile: (650) 839-5071

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